
Tektronix TDS 7404 Digital Phosphor Oscilloscope
DPO
HORIZONTAL
TRIGGER
PROBE COMPENSATION
AUX IN
AUX OUT
SIGNAL OUT
Intro to
Signal Processing

Agenda

- Measurements with Photo-Multiplier Scintillation Detectors

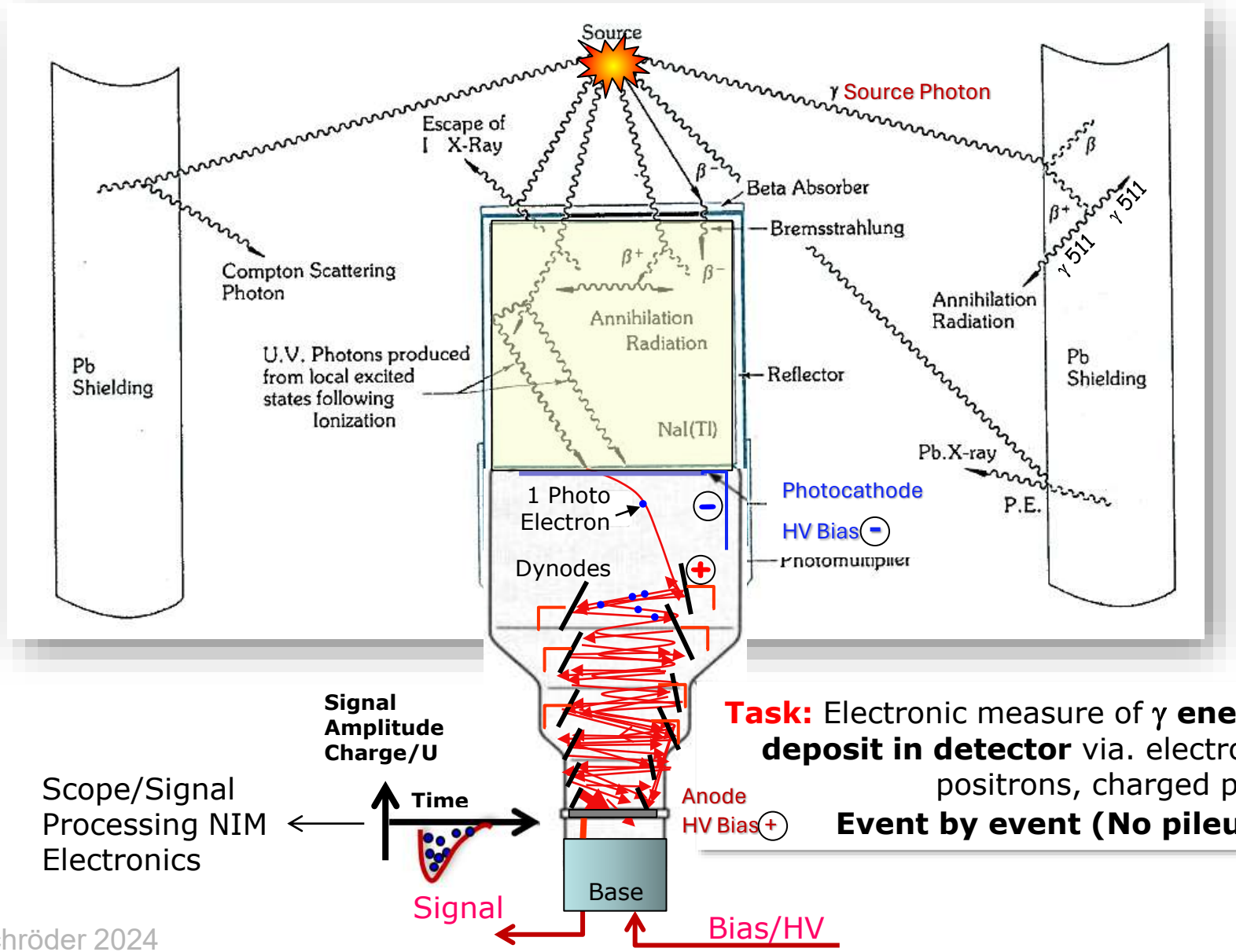
- Electronic signal processing, scintillation detectors
- Fast-Slow electronic circuits
- Display with oscilloscope, front panel, signal traces
- NIM modules for analog and digital branches
  - Discriminator, timing single channel

- DDC-8 data acquisition system
  - Analog vs. digital timing
  - Analog-to-digital signal conversion (ADC)
  - Event data stream
  - Frequency spectrum histogram, energy calibration

Take Radiation-Safety class/exam

Next: Igor exercises with γ spectra

Measurements with Scintillation Detectors

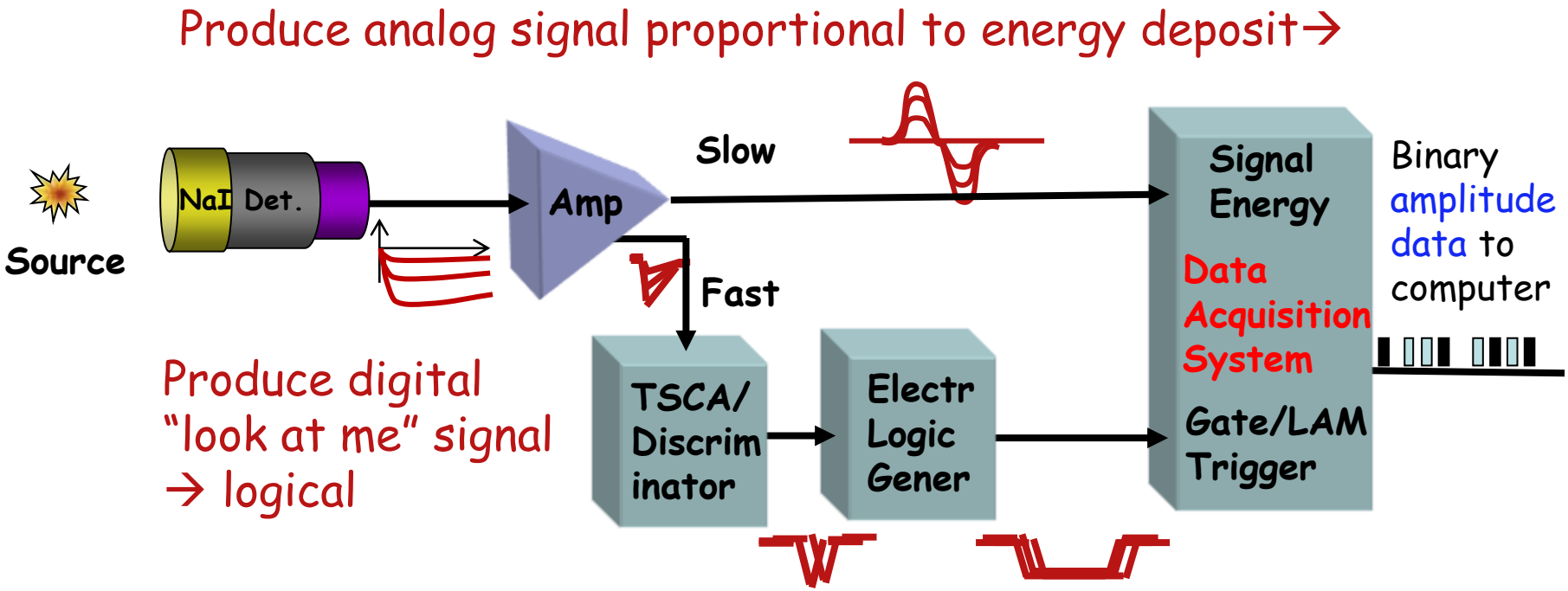


Task: Electronic measure of γ **energy deposit in detector** via. electrons, positrons, charged part.
Event by event (No pileup!)

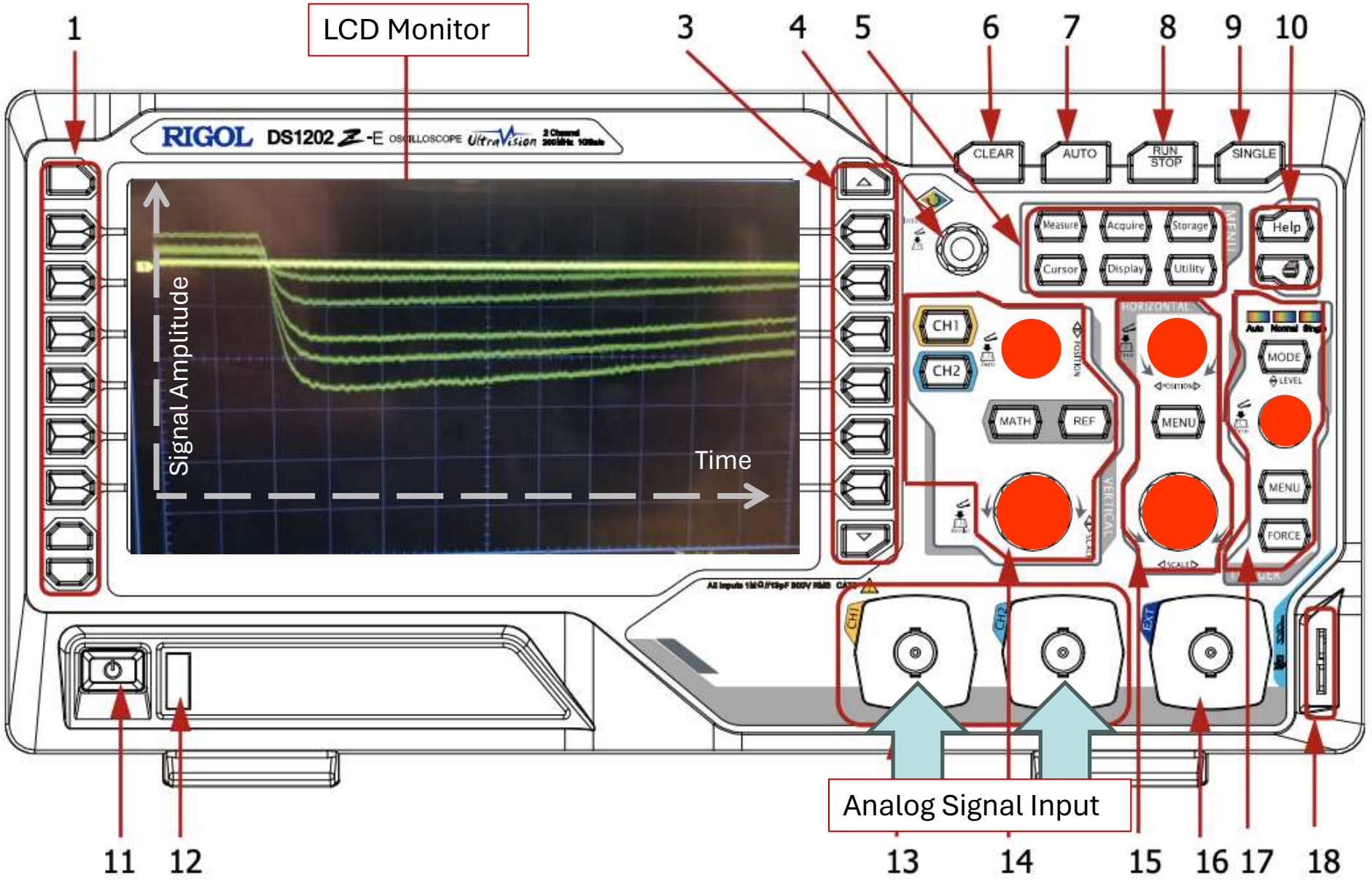
Principle of Fast-Slow Signal Processing

Two branches of signal processing:

1. Fast logic branch: Produce unitary, "logical" signal indicating that detector had one acceptable event, further use in fast decision making (accept/reject)
2. Slow analog branch: Integrate, amplify, and shape original detector energy signal to match requirements of analytical electronics modules and computer data acquisition/storage system.



Signal Oscilloscope Front Panel



Signal Oscilloscope Front Panel Descriptions

No.	Description	No.	Description
1	Measurement Menu Softkeys	10	Help/Print
2	LCD	11	Power Key
3	Function Menu Softkeys	12	USB Host Interface
4	Multifunction Knob	13	Analog Channel Input Area
5	Common Operation Keys	14	VERTICAL Control Area
6	CLEAR	15	HORIZONTAL Control Area
7	AUTO	16	External Trigger Input
8	RUN/STOP	17	TRIGGER Control Area
9	SINGLE	18	Probe Compensation Signal Output Terminal/Ground Terminal

Terminate input signal by 50Ω for NIM logic pulses.

Trigger Menu for time sweep condition: Trigger channel #, rising/falling level, AC vs. DC.

Adjust display ranges and zero for horizontal (time) and vertical (signal amplitude) scale.

Adjust trigger signal (discriminator) level.

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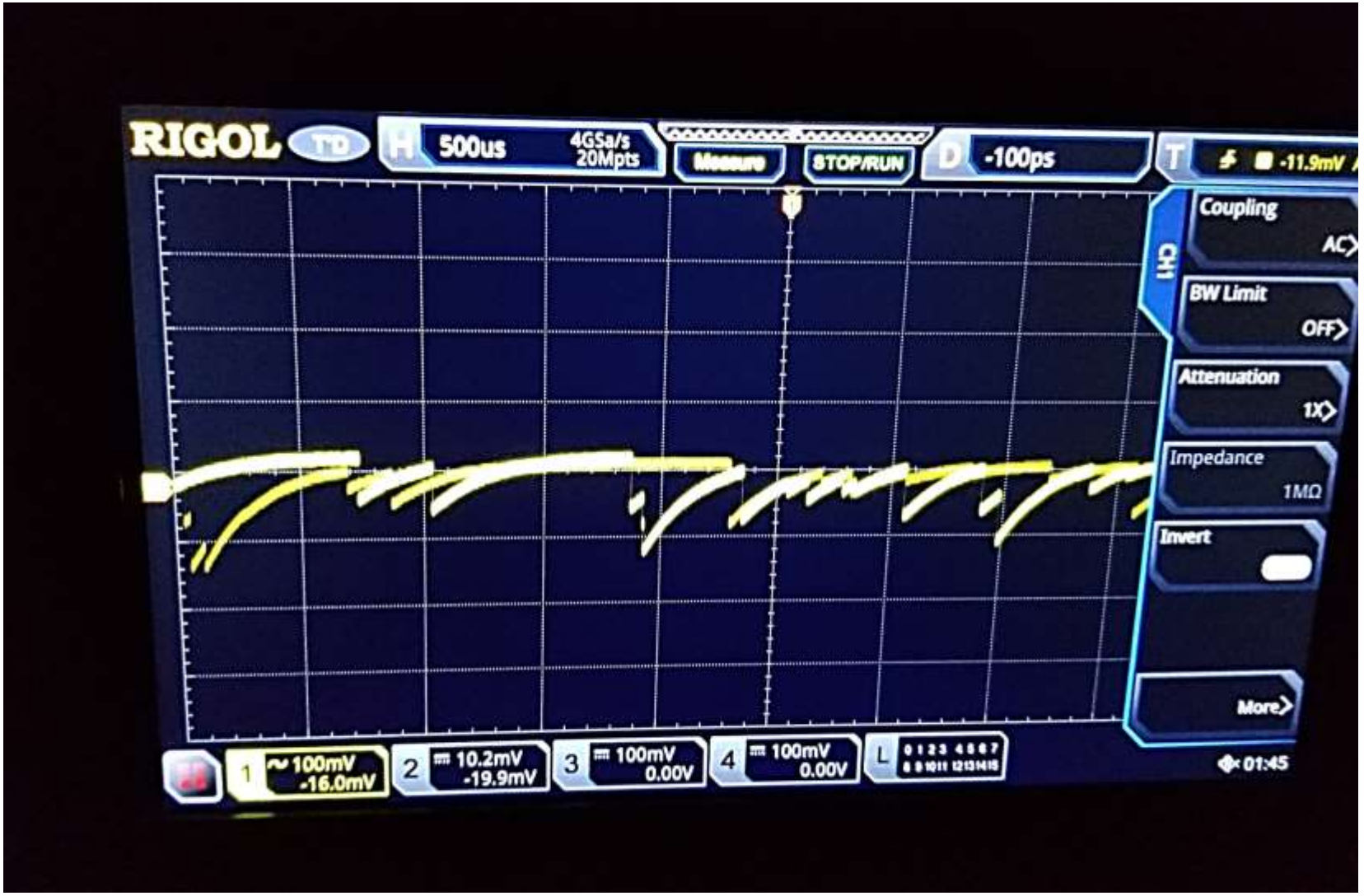
Signal Output from PM Base



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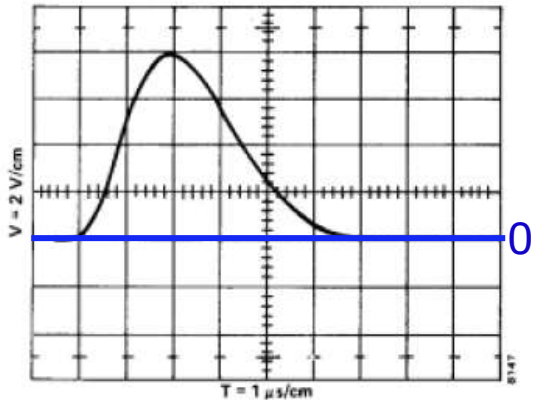
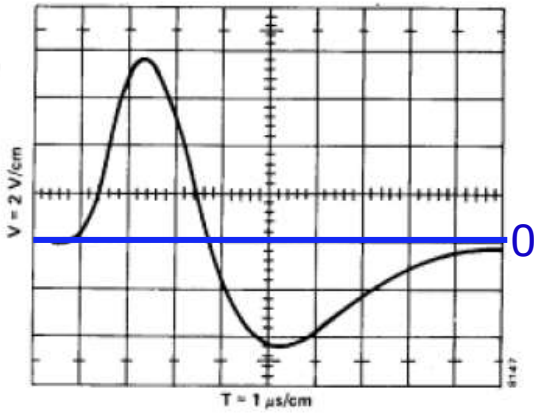
Analog Branch Elements: Slow Analog Signal Amplifiers

Uniform signal shape for all→ Amplitude ~ Energy



Correct Amplifier Unipolar Output.



Correct Amplifier Bipolar Output.

Tasks: Generate signal with amplitude **proportional** to collected detector charge. Needs absolute calibration of pulse amplitude.

← **Preamp Power**

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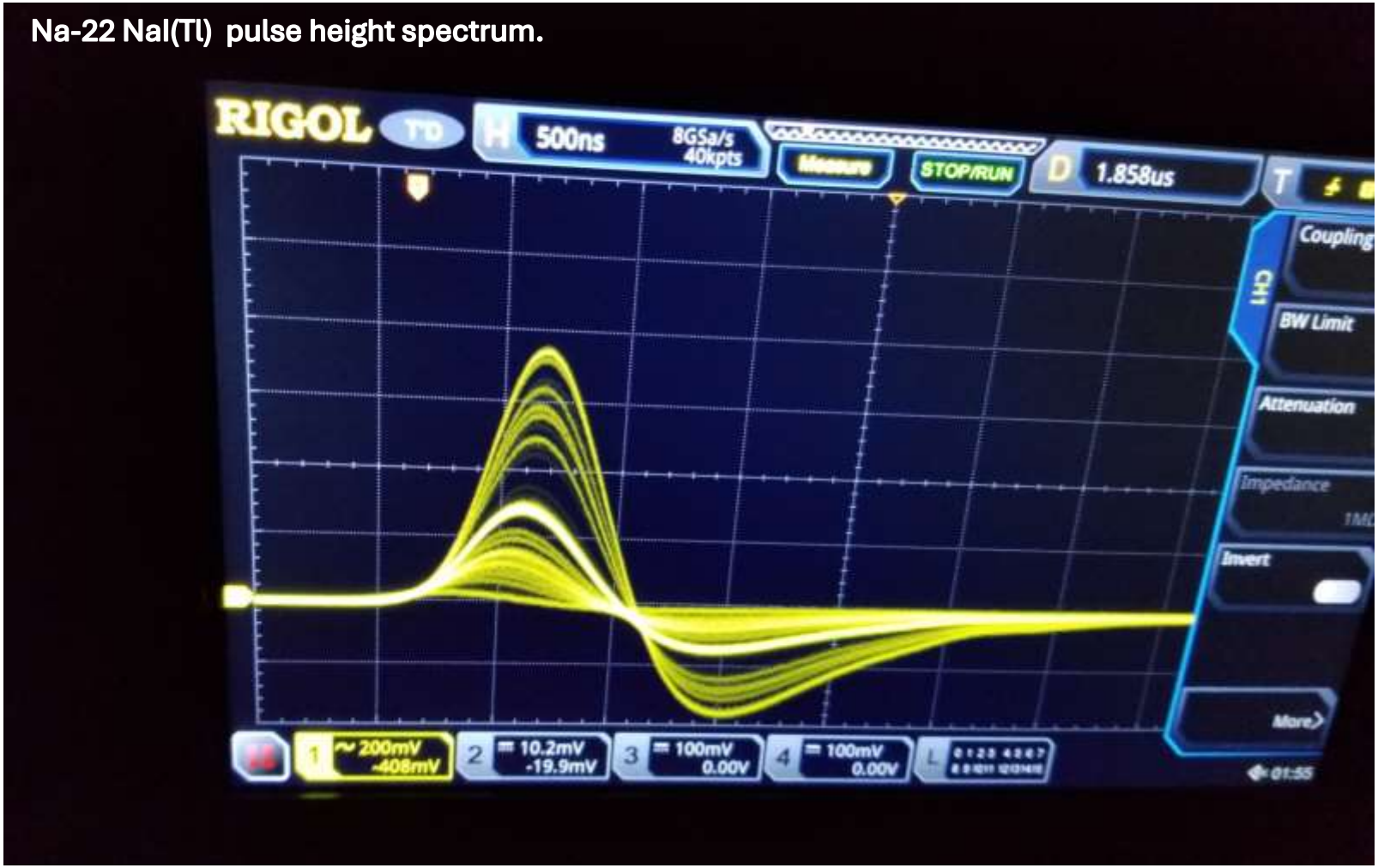
Signal Output Main Amplifier



NaI(Tl) detector with Na-22 source. Display of a superposition of several 10s of individual events: Amplifier signal amplitude (200mV/cm) vs. time (500ns/cm).

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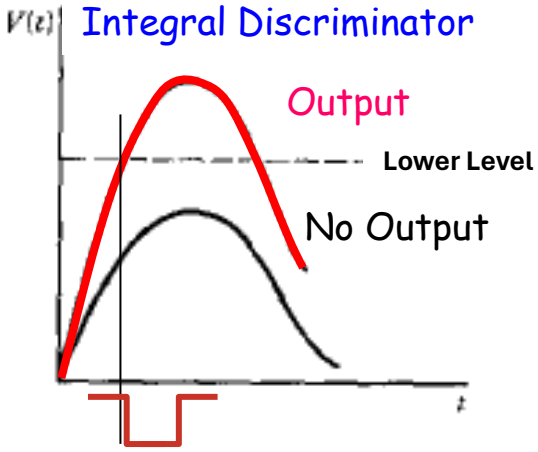
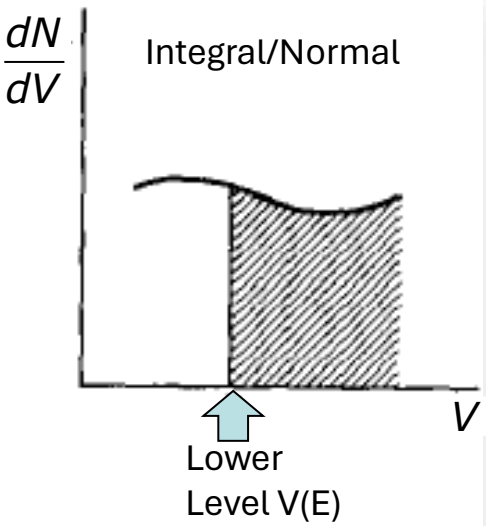
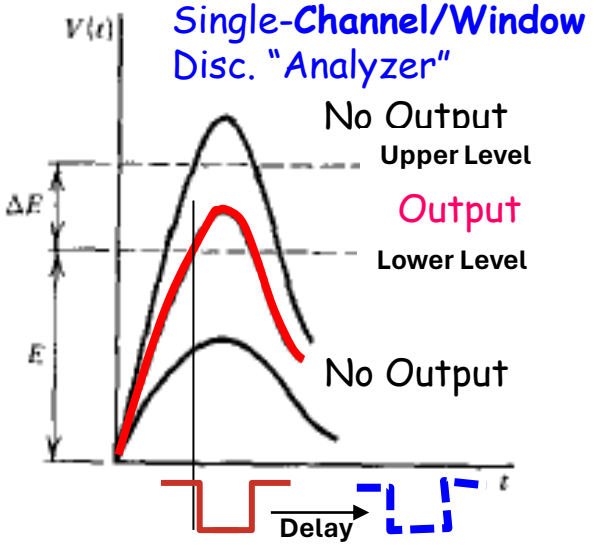
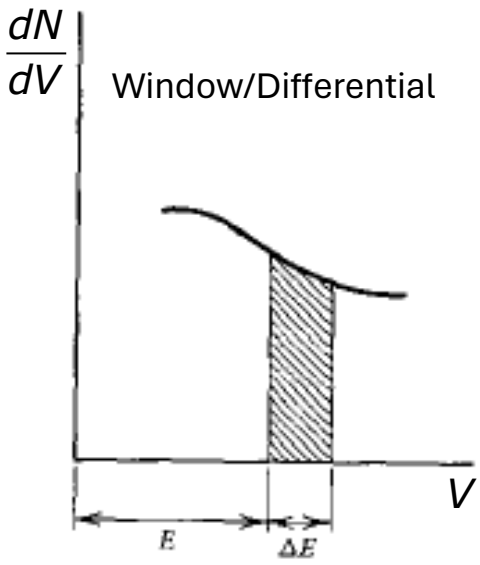
Leading-Edge Discriminator: "Single Channel" TSCA

Tasks: Indicate presence of event, define "time-zero" t_0

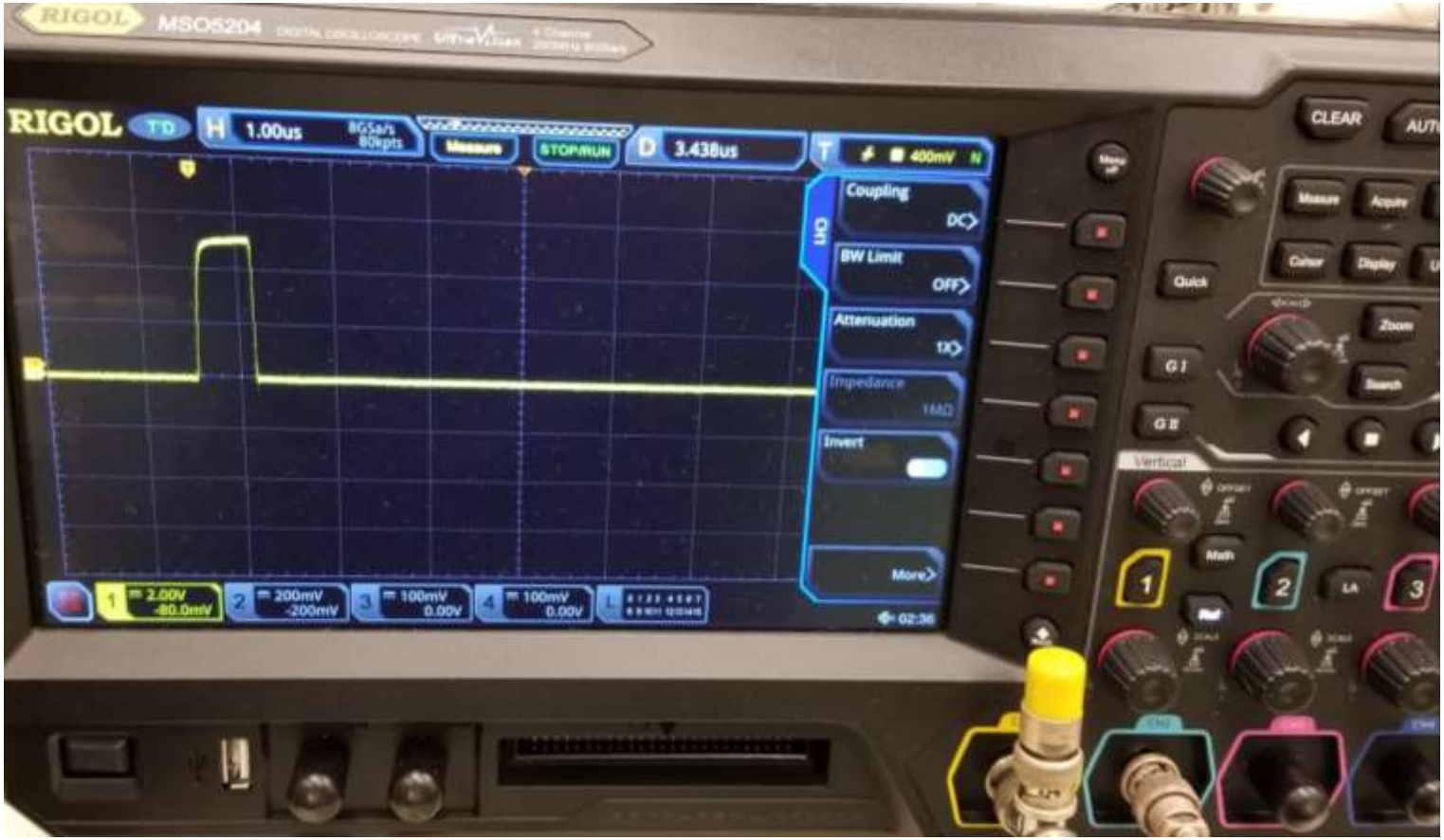








Logic Branch: NIM/TTL Signals



Logic signals =Discriminator output pulses, have a constant shape, independent of shape and amplitude of input signals from detector.

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Digital Sampling Oscilloscope

Displaying the time dependent signal amplitude U(t)
Sweep an illuminated trace U(t) horizontally along the screen

Signal Trigger Level Adjust

Output media for screen shots (USB/Disc)

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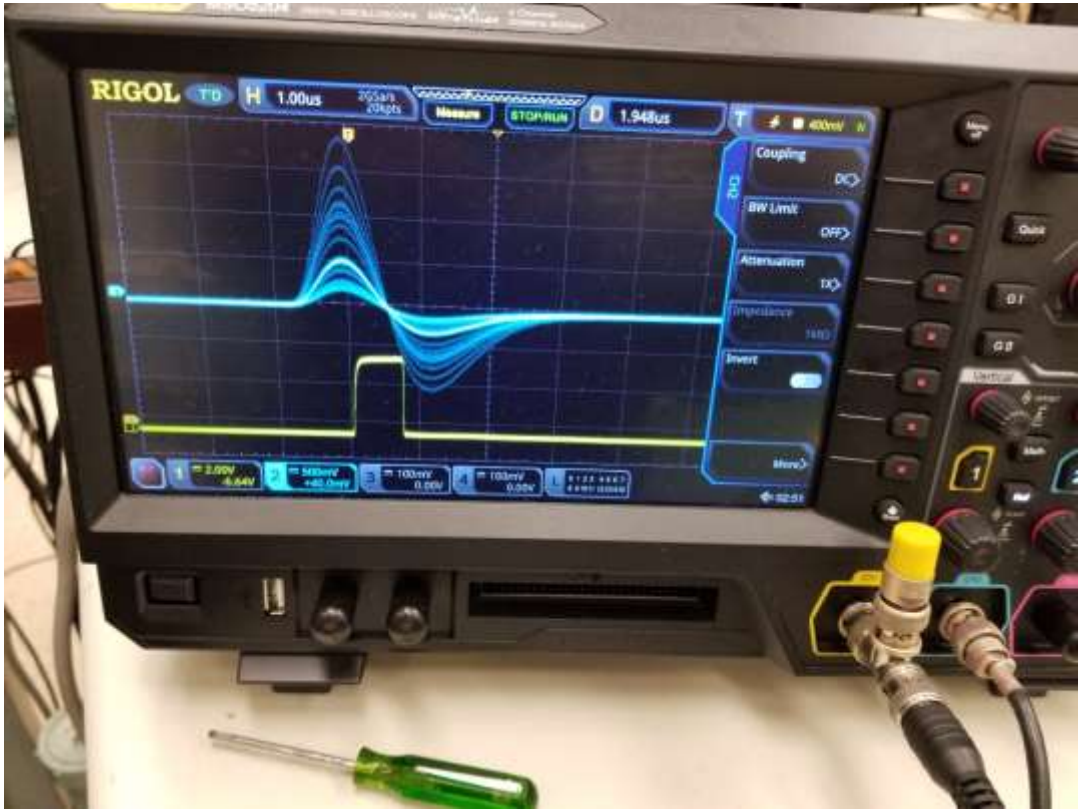

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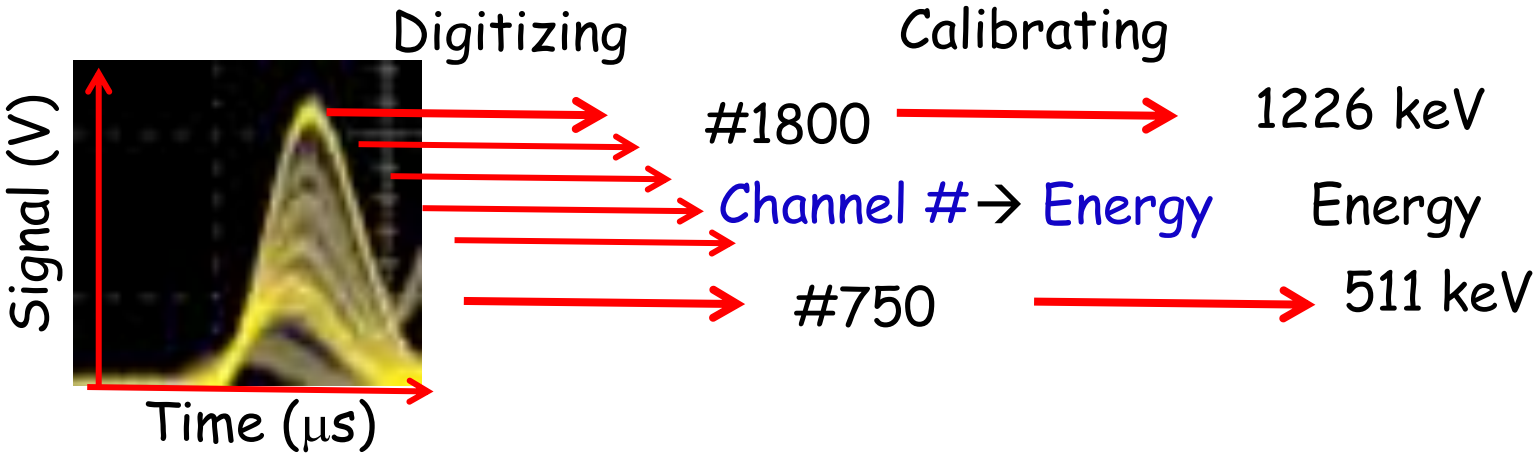
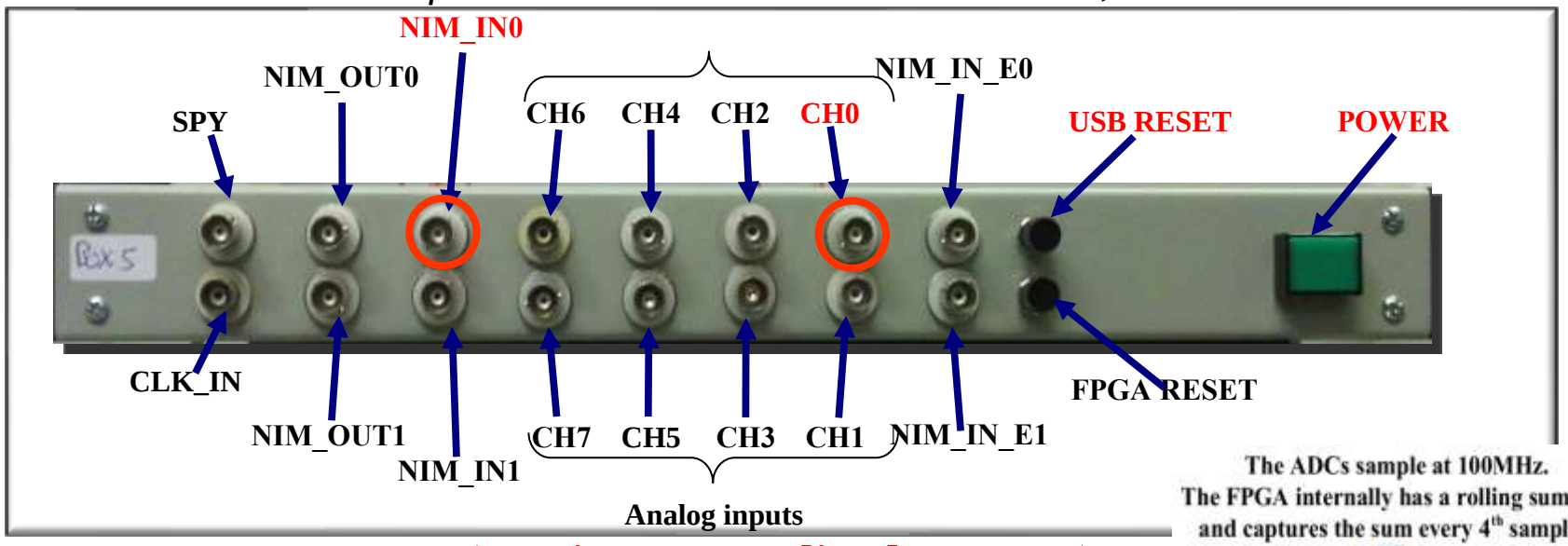
Data Acquisition with DDC-8 Digitizer



$2048 = 2^{11} \rightarrow +2V \triangleq$ *full scale* $\rightarrow +1.0V \triangleq 10\,000\,000\,000, +1.5V \triangleq 11\,000\,000\,000$



+/- 1V (maximum amplitude = 2V !!)

The ADCs sample at 100MHz.
The FPGA internally has a rolling sum of 4 and captures the sum every 4th sample.

Effective sampling = 25MHz
(1 sample covers 40ns)

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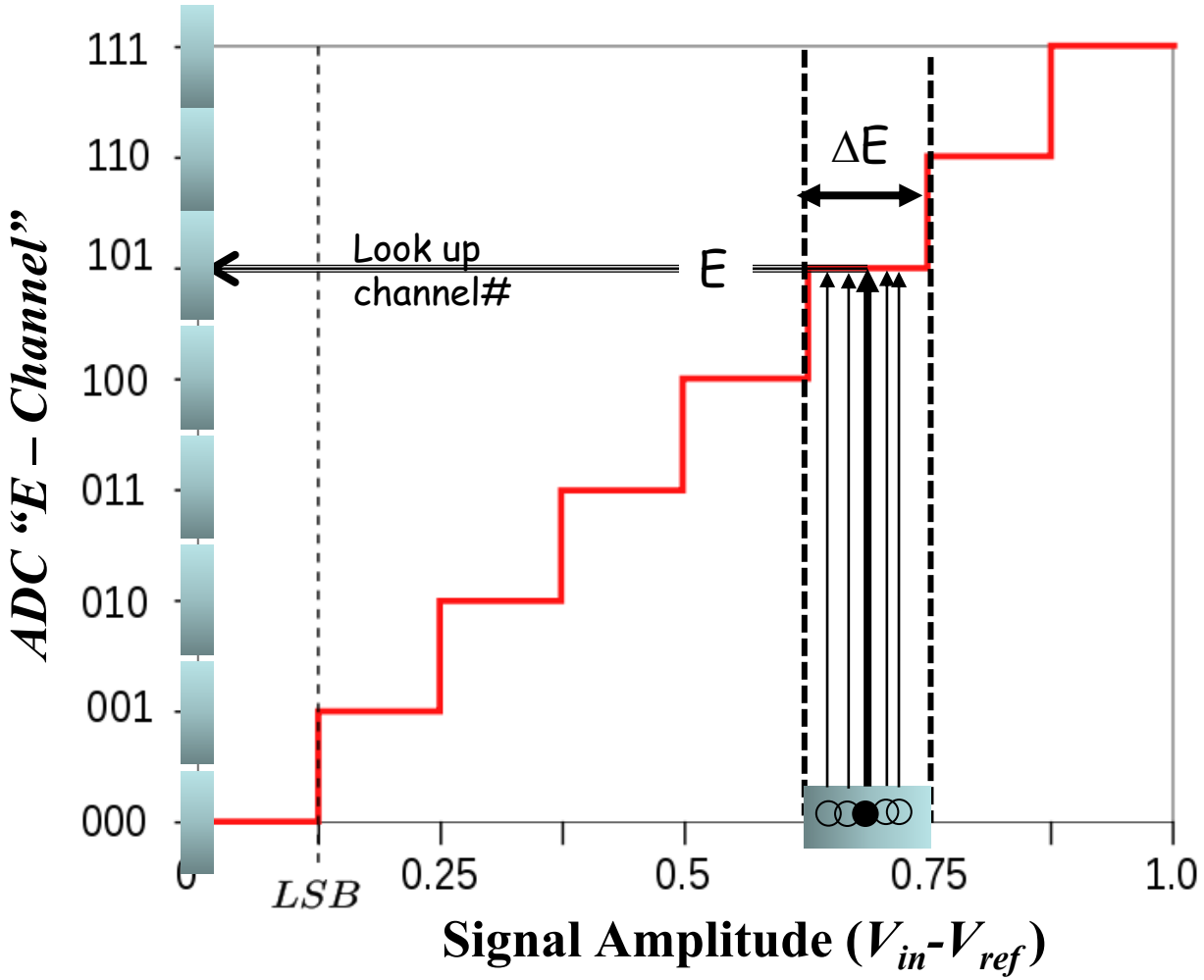
Analog-to-**D**igital **C**onverter (ADC) Principle of Operation



Divide total range of signal amplitudes into ADC "E channels" (bins) of fixed width ΔE → event counters. Input signal triggers (initiates) comparator channel scan.

More bins →higher resolution

Typical # of channels per ADC: 1k=1024 2k,…, 8k.

Event signal amplitude → binary number = ADC# → I(ADC#) ← I(ADC#)+1
Accumulated I(ADC#) = Pulse (signal) height spectrum

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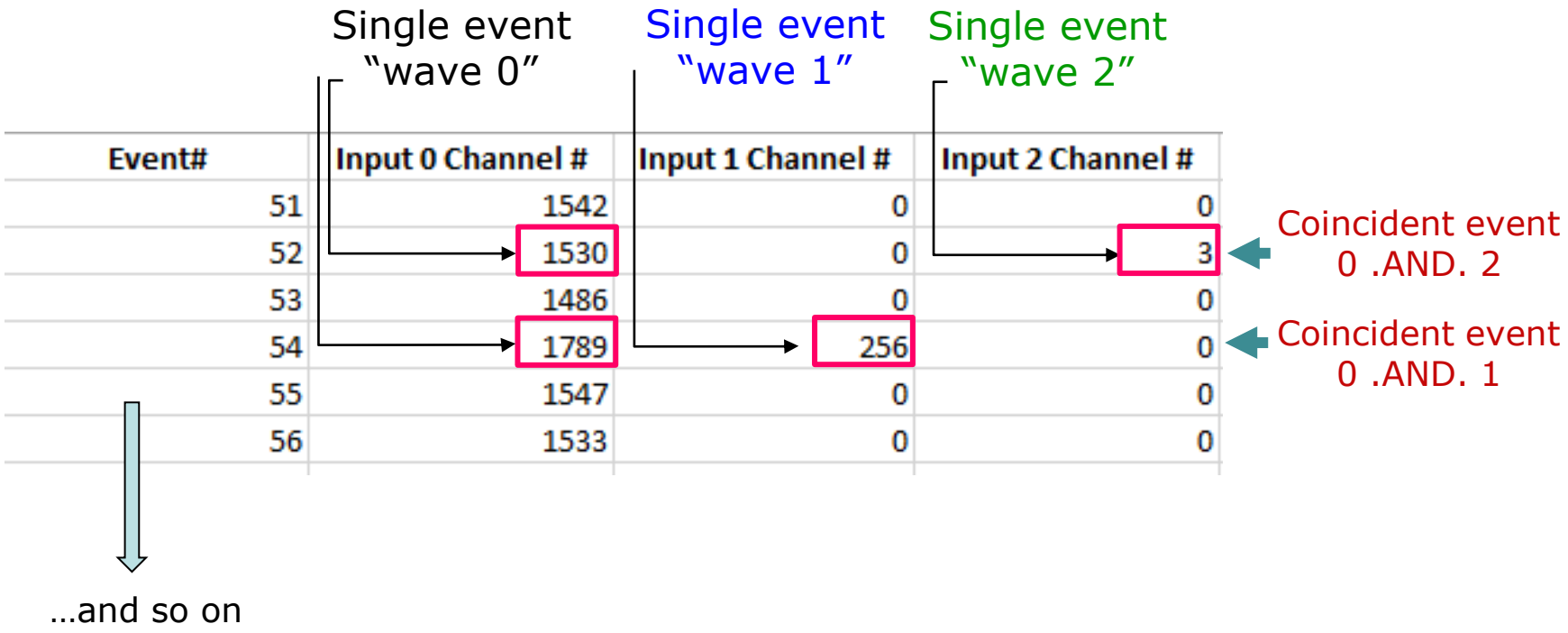
Digital Event Data Stream

Example of event stream with signals (observables) measured in 3 inputs of Data Acquisition Module (DDC-8),
Sample displays 6 successive events.



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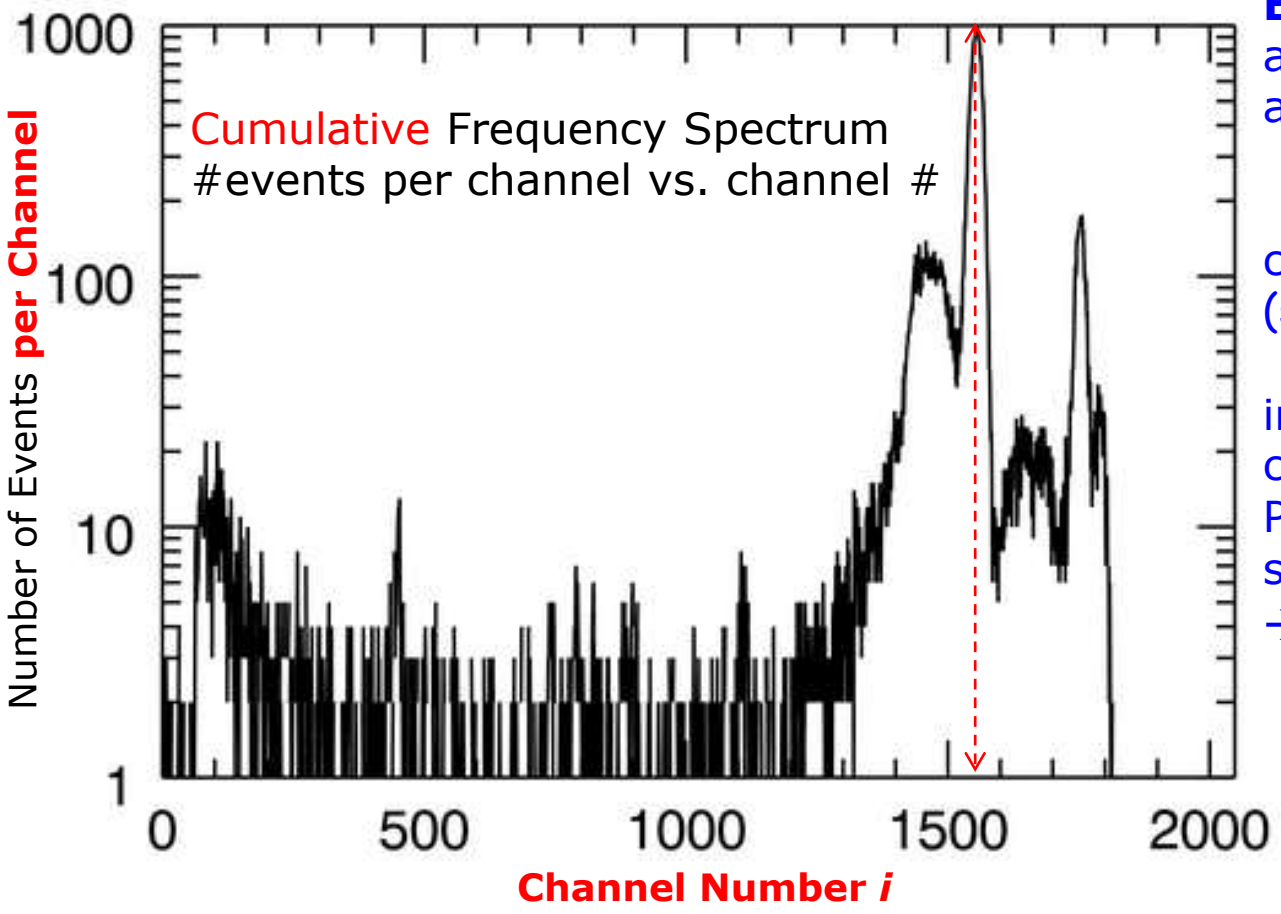
Histogram of Pulse-Height (Amplitude) Spectrum



Each event provides 1 analog signal amplitude V_{in} →
→ digitize V_{in}

channel numbers i (V_{in})
(segment of PC memory)

increment (add +1) content ($N_i \rightarrow N_i + 1$) of PC cell # =start of spectrum + channel #i.
→ F m

Calibrations :

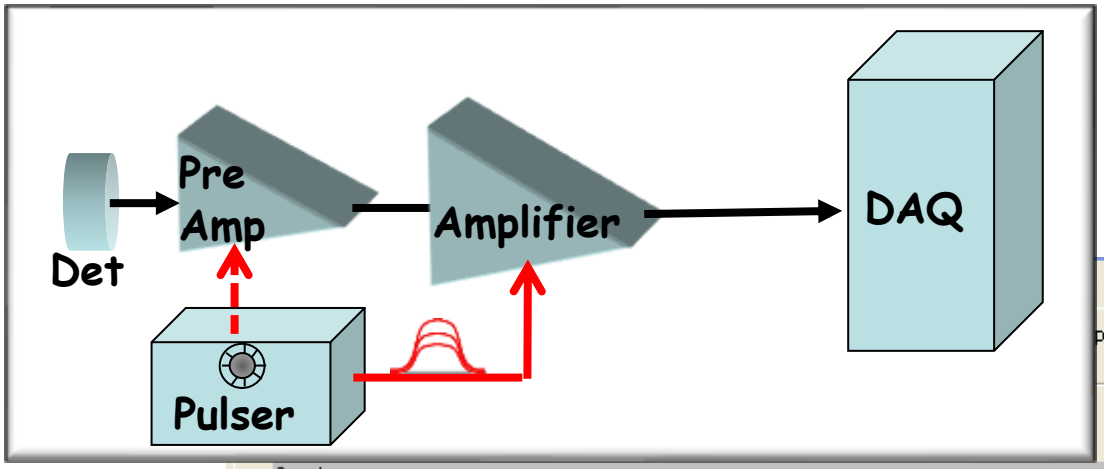
$$i(V) = i_0 + \frac{\Delta i}{\Delta V} \cdot V$$

$$E(i) = E_0 + \frac{\Delta E}{\Delta i} \cdot i$$

$$\textit{Measured}: \frac{\textit{Number of events } \Delta N}{\textit{ADC} - \textit{channel}} \left(\textit{unit} = \frac{\textit{counts}}{\textit{channel}} \right) \rightarrow \frac{dN}{dE} \left(\textit{unit} = \frac{\textit{counts}}{\textit{keV}} \right)$$

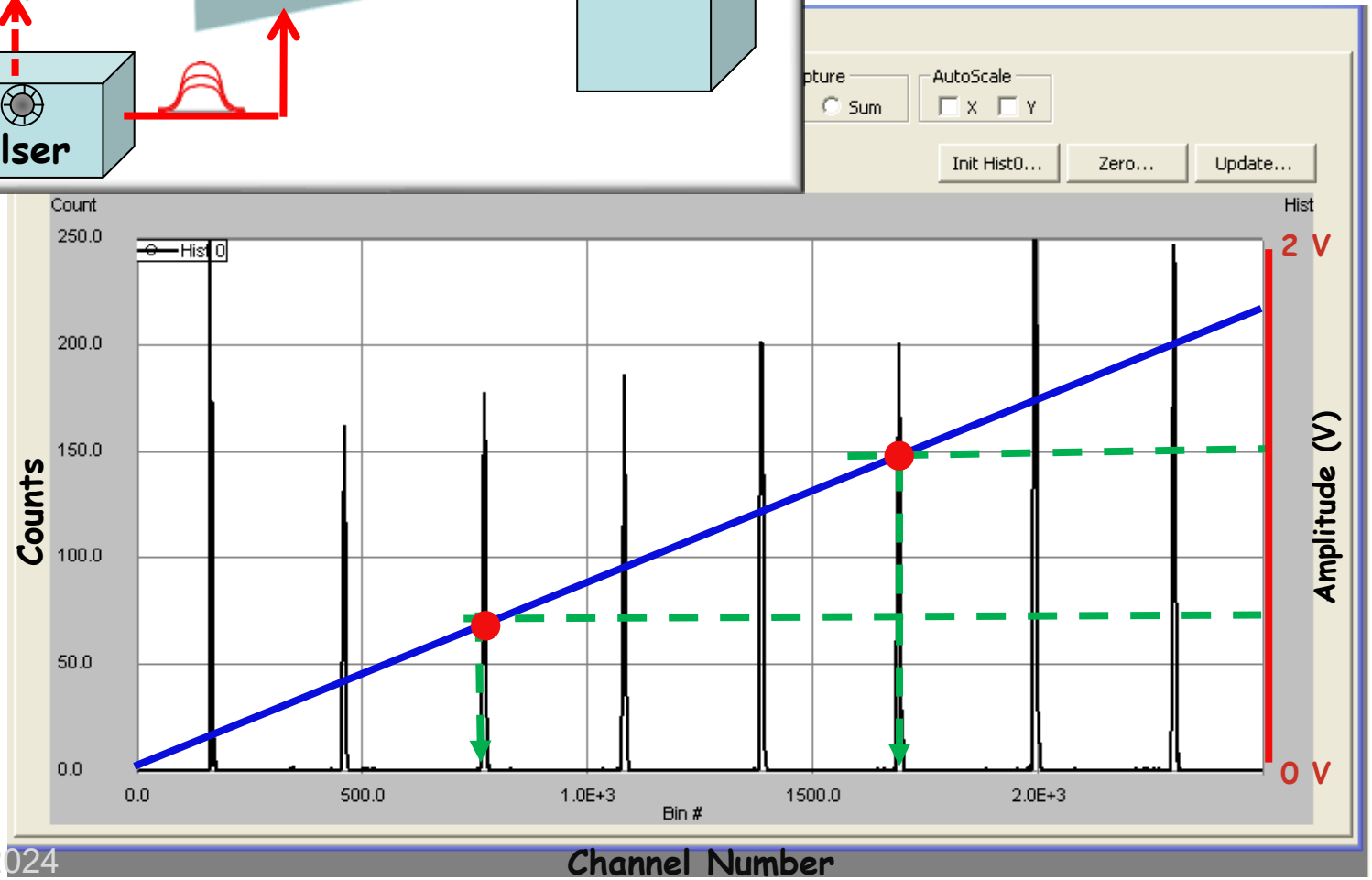
$$\textit{Total number of events}: N = \sum_{i=1}^{2k} \left(\frac{\textit{Number of events } \Delta N_i}{\textit{ADC} - \textit{channel}_i} \right) \rightarrow \int_0^{\infty} \left(\frac{dN}{dE} \right) dE$$

Amplifier/ADC Linearity Check: "Pulser Calibration"



Series of signals from calibrated **precision pulser generator** fed into slow circuit.

"Pulser Fence" calibrates abscissa of DAQ (Channel, Bin#) in Volts, MeV, etc.



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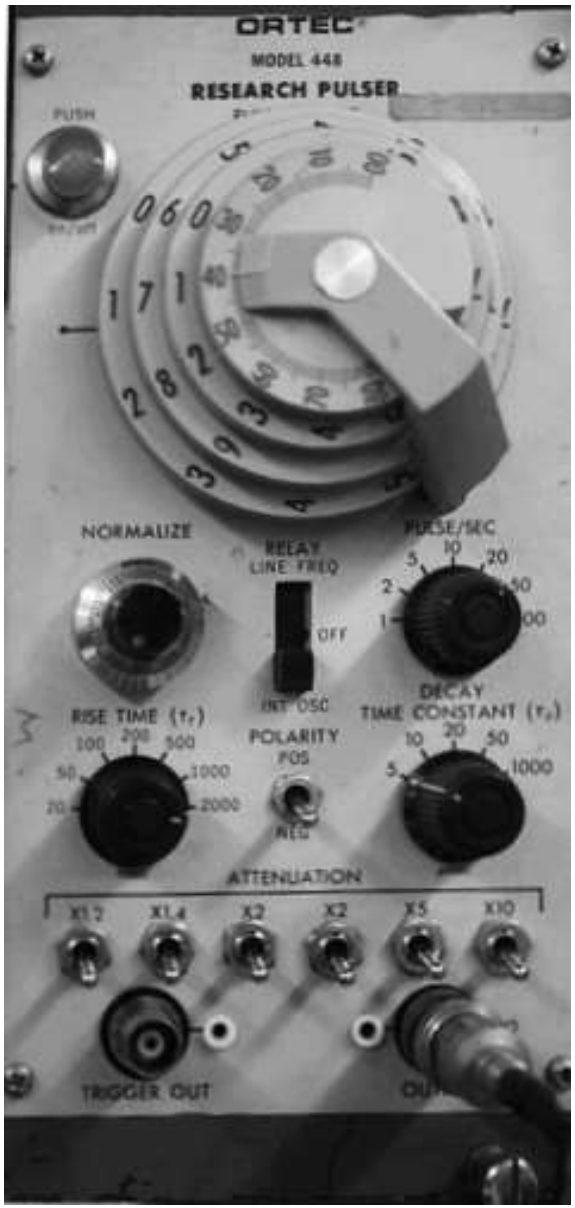
Precision Pulse Generators



Popular ORTEC spectroscopy-grade precision pulse generators. Other brands: BNC, Tennelec, Canberra,..

Output signal amplitude is highly stable and varies linearly with dial/switch settings.

Output pulse amplitude is calibrated independently in units of Volts, keV, etc.

End of Intro Signal Processing

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